AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [00028] with the following amended paragraph:

[00028] Figure 4 illustrates how an interpreter may work with a mixed stack in an exemplary embodiment of the invention. In an exemplary embodiment of the invention, an instruction, such as a bytecode instruction may undergo a stack-state aware translation into threaded code, which may indicate an entry point into ~~shared~~ cascading execution code for executing the instruction.

Please replace paragraph [00029] with the following amended paragraph:

[00029] Figure 4 depicts an exemplary embodiment of a transition 400 of an instruction from bytecode, for example, to ~~shared~~ cascading execution code. As shown in Figure 4, prior to interpreting a method the first time, a bytecode instruction 401 may be passed to or interpreted by a stack-state-aware translator 402. The stack-state-aware translator 402 may produce threaded code 403. Based on the threaded code 403, the instruction 401 may be dispatched according to the operand stack state of the instruction. In an exemplary embodiment of the invention, when an instruction is dispatched according the operand stack state of the instruction, the entry point into ~~shared~~ cascading execution code 404 may be determined and the instruction may be executed from that entry point.